Remarks/Arguments:

Claims 1-20 are pending in this application. Claim 10 has been amended. No new material is introduced herein.

Claims 1-3 and 9-16 were rejected under 35 U.S.C. § 102(e) as being anticipated by Zhao et al. (U.S. Patent No.6,727,946). Claims 4-8 were rejected under 35 U.S.C. § 103(a) as being obvious in view of Zhao and Chi (U.S. Patent No. 5,854,100). Claims 18-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chi (U.S. Patent No. 5,854,100). Applicants request reconsideration. In particular, neither Zhao nor Chi, nor their combination, disclose or suggest "a bias circuit operable to apply voltages across the pixels to induce carrier injection into the photodiode regions to reduce image lag," as required by claim 1. Claim 18 includes a similar recitation.

Zhao discloses an active pixel sensor reset circuit for reducing image lag. Specifically, Zhao's circuit is intended to reduce image lag by "pulling down" the sensor potential SP1 before soft reset. See Fig. 4 and column 6, lines 4-6. As shown in Fig. 4, biasing circuit 320 is used to quickly pull down sensor potential SP1. Examiner contends that biasing circuit 320 is "operable to apply voltages across the pixels to induce carrier injection into the photodiode regions." However, biasing circuit 320 is not operable in that manner.

Biasing circuit 320 is operable to apply a bias signal to loading transistor M4. In this way, biasing circuit 320 is only operable to create a path between M4 and SP1. As shown in Fig. 4, M4 is connected to ground. Thus, even when a path is established between M4 and SP1, biasing circuit 320 is only operable to pull SP1 down to ground. It is <u>not</u> operable to apply a voltage across sensor S1 because, when circuit 320 is active, both sides of the photodiode will be at ground potential. Therefore, biasing circuit 320 is <u>not</u> operable to induce carrier (electron) injection into the photodiode regions. Thus, Zhao does not include all the features of claim 1.

Chi discloses an active pixel sensor reset circuit for reducing image lag. Relevantly, the circuit includes a photodiode D1, a P-MOS transistor M1 and a bipolar transistor Q1. See Fig. 5. Light impinging on photdiode D1 imparts sufficient energy to create electron-hole pairs in the photodiode D1. Excess electrons are removed through power supply voltage Vcc. The charge remaining in photodiode D1 is then read out by turning on P-MOS transistor M1, causing the

charge to flow into transistor Q1. This will forward bias bipolar transistor Q1 and cause the charge to be amplified. The amplified charge will flow into the sense amplifier 425. This charge represents the amplitude of light impinging on the photodiode D1. A remnant of minority carriers (electrons) remain in transistor Q1 from electrons injected from forward biasing transistor Q1 during the read operation. Thus, Chi discloses injecting electrons into the bipolar transistor and not the photodiode. Therefore, because claims 1 and 18 recite that carriers are injected into the photodiode regions, Chi does not disclose all the features of claims 1 and 18.

Moreover, Chi teaches away from inducing carrier injection into the photodiode regions because it states that the minority carriers can not flow through the interverter/P-channel MOS transistor M1 to reach the photodiode. It is clear that Chi is addressing a different problem: image lag caused by the bipolar transistor.

Because neither Zhao nor Chi, nor their combination, disclose or suggest these limitations of claims 1 and 18, claim 1 is not subject to rejection under 35 U.S.C. § 102(e) as being anticipated by Zhao and claim 18 is not subject to rejection under 35 U.S.C. § 102(b) as being anticipated by Chi. Claims 2 and 9-10 depend from claim 1; claims 3 and 5 depend from claim 2; claim 4 depends from claim 3; claims 6 and 8 depend from claim 5; claim 7 depends from claim 6 claims 11 and 15-16 depend from claim 10; and claims 12-14 depend from claim 11. Accordingly, these claims are not subject to rejection under 35 U.S.C. § 102(e) as being anticipated by Zhao nor are they subject to rejection under 35 U.S.C. § 103(a) as being obvious in view of Zhao and Chi for at least the same reasons as claim 1, from which they depend. Claims 19 and 20 depend from claim 18. Accordingly, these claims are not subject to rejection under 35 U.S.C. § 102(b) as being anticipated by Chi for at least the same reasons as claim 18, from which they depend.

Claim 17 was rejected under 35 U.S.C. § 103(a) as being obvious in view of Zhao and Baer (U.S. Patent No. 6,914,230). Applicants request reconsideration. In particular, Baer is not prior art under 35 U.S.C. § 103(c) because, at the time the above-referenced application was filed, both the subject application and the Baer reference were assigned to Agilent Technologies, Inc. Additionally, claim 17 depends from 10, which depends from claim 1. Accordingly, because Baer is not prior art under 35 U.S.C. § 103(c), claim 17 is not subject to rejection under 35 U.S.C. § 103(a) for at least the same reasons as claim 1, from which it depends.

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Reply to Office Action of 11/01/2006

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Claim 10 was objected to as being of improper dependent form and claims 11-17 were objected to because they depend on an claim being of improper dependent form. Claim 10 has been amended so that it now properly depends from claim 1. Withdrawal of this objection and withdrawal of the objections to claims 11-17 is respectfully requested.

In view of the foregoing amendments and remarks, Applicants request that the Examiner reconsider and withdraw the rejection of claims 1-20.

Respectfully submitted,

Kenneth N. Nigon, Reg. No. 31,549
Attorney for Applicants

KNN/drm/mc

Dated: February 1, 2007

P.O. Box 980
Valley Forge, PA 19482
(610) 407-0700

The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. (571) 273-8000) on the date shown below.

Melissa Clemons 2/1/07

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